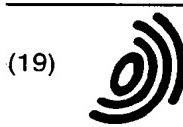


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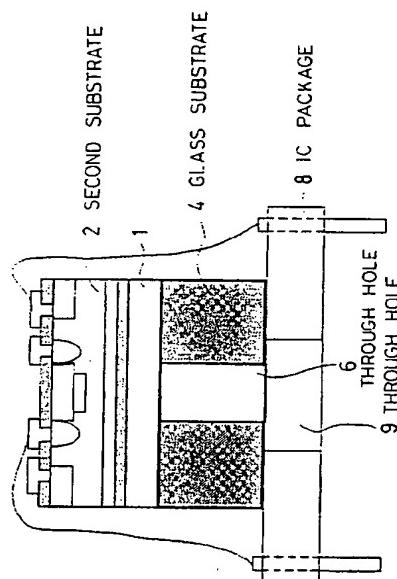
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London WC1R 4JH (GB)(54) **Avalanche photodiode joined with an integrated circuit package and method of fabrication**

(57) An avalanche photodiode to detect X-rays comprising a shallow depletion layer on a FZ-SOI substrate (1, 2). The substrate and a glass substrate (4) are joined with anode junction and the glass substrate is joined with an IC package (8) using eutectic crystal joining process free from degassing. The lead pin (10) of the IC package is connected to an electrode (11) formed on the glass substrate.

FIG. 6



EP 0 697 743 A1

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## Description

The present invention relates to an avalanche photodiode that can be used for light detection, X-ray detection and electron beam detection or the like, and to a method for fabricating the same.

Heretofore, avalanche photodiodes use a semiconductor substrate on which an epitaxial  $\pi$  layer 21 is provided which is formed by epitaxially growing silicon on a floating zone (FZ) substrate 20 as shown in Fig. 20. Further, as shown in Fig. 22, a thickness  $d$  which comprises part of a FZ substrate may be set to several tens of  $\mu\text{m}$  for usage. Such a semiconductor substrate is directly joined with an IC package as shown in Figs. 21 and 23, and electrodes 3a and 3b are bonded to a lead pin 10 of the IC package with a metal wire 15 to provide an electric conduction.

The conventional avalanche photodiode assumes the above-mentioned semiconductor substrate structure, but the following points can be raised as problems that should be solved.

When an FZ epitaxial substrate structure is adopted, there is a problem in that firstly an oxygen content in the substrate is small, so the physical strength of the substrate is weak, so that deformation (warp in a wafer) is generated in the substrate under heat treatment in the fabrication step, and dislocation slip increases, which makes it difficult to continue the subsequent processes and which deteriorates the device characteristics thus fabricated.

Further, secondly, when the X-ray or the like is detected with the avalanche photodiode, a P<sup>+</sup>-layer comprising a FZ substrate 20 shown in Fig. 20 constitutes a incident light scattering area so that the width of the area should be as short as possible. To reduce the contact resistance with the electrode 22, a width of at least several  $\mu\text{m}$  is required for the layer. In addition to a current generated in the depletion layer when the X-ray is incident, there also exists a current which is generated by the delayed depletion of carriers generated in this area to the depletion layer. Thus there is a problem that the time resolution of the avalanche photodiode reduces.

When an FZ substrate having a thickness of about tens of  $\mu\text{m}$  is used and the thickness of the P<sup>+</sup>-layer 20 shown in Fig. 22 is thin, the above-mentioned problem of the time resolution can be avoided. However, since the substrate is thin, the physical strength thereof is weaker than the normal FZ substrate. So the result that problems become more serious as seen in the reduction in the fabrication yield ratio resulting from an increase in the warp of the wafer caused by heat treatment process and a dislocation slip and a reduction in the device performance such as an increase in the reverse bias leak current.

When the P<sup>+</sup>-layer 20 is formed after part of the FZ substrate 27 is etched or polished to be thinned down to a thickness of tens of  $\mu\text{m}$  like the conventional example shown in Fig. 22, the above-mentioned problems of the

mechanical strength and the time resolution are improved. However, it is difficult to control with a good precision the thickness  $d$  of the remaining silicon wafer with the result that the planarity and the crystallinity of the silicon surface 23 are far from the counterparts of the original wafer surface. When the silicon is dry etched, the silicon surface becomes extremely rough and crystal defects caused by the damage at the time of etching are introduced. When the silicon is wet etched, an etch pit

or the like is likely to be generated. Consequently, the performance of the device formed there is deteriorated.

Examples in which the above-mentioned avalanche photodiode is packaged are shown in Figs. 21 and 23. The physical strength of the avalanche photodiode is weak even when the diode is directly packaged in the IC package. Thus there arises a problem in that the diode is sometimes broken when the diode is wire-bonded, the substrate is deformed (a warp in the wafer), and the device characteristics of the fabricated device are deteriorated. Additionally, when the diode is used in the atmosphere of a high temperature, the influence of heat to the avalanche photodiode by heat accumulation of the IC package largely deteriorated the characteristics of the avalanche photodiode.

An object of the invention is to provide a X-ray detecting device having a good detection sensitivity and a good time resolution.

Means adopted in the present invention to attain the above-mentioned object is an avalanche photodiode comprising:

a first insulating film formed on a first substrate;  
a second substrate comprising a floating zone silicon semiconductor substrate which is crystal grown on said first insulating film;

a PN-junction formed on said second substrate;  
a plurality of electrodes for applying a voltage to said PN-junction which is formed on said second substrate;  
wherein said first substrate is joined with a glass substrate, the surface of the glass substrate is joined with an integrated circuit package, and said plurality of electrodes are electrically connected with a lead pin of the integrated circuit package.

Further, the present invention provides an avalanche photodiode comprising:

a PN-junction formed on a second substrate;  
a plurality of electrodes for applying a voltage to said PN-junction; wherein the surface of said second substrate on which said plurality of electrodes are formed is joined with the surface of a glass substrate on which a second electrode is formed, said plurality of electrodes and said second electrode on the glass substrate are electrically connected to each other, the surface of the glass substrate opposite to the surface where the second electrode is formed is joined with an integrated circuit package, and said second electrode formed on the glass substrate is electrically connected to the lead pin of the integrated circuit package.

The plurality of electrodes can be formed by sandwiching a second insulating film.

Further, the present invention provides a method for fabricating an avalanche photodiode comprising the steps of:

- (a) forming a metal thin film on one side of a glass substrate;
- (b) patterning said metal thin film;
- (c) etching said metal thin film by using a patterned photoresist as a mask;
- (d) etching said glass substrate with a fluoric acid agent by using said metal thin film as the mask; and
- (e) removing the photoresist and the metal thin film used as a mask, and processing a glass cover for protecting the surface of a floating zone substrate;
- (f) protecting the floating zone substrate by opposing an etched surface of said glass cover to a floating zone substrate of a silicon on insulator substrate on which the avalanche photodiode is formed to join the floating zone substrate with a portion of the glass cover where the metal thin film is removed;
- (g) forming a diaphragm by etching with an alkaline agent a portion of the silicon on insulator substrate where a silicon nitride film is removed to terminate the progress of etching with a silicon oxide film in the silicon on insulator substrate;
- (h) dicing a thin portion of the etched portion of the glass substrate from the side of the glass substrate to a depth such that the glass substrate is not penetrated; and
- (i) dicing a portion of the silicon on insulator substrate located at a relative position with the dicing line which is processed on said glass substrate to a depth such that the silicon on insulator substrate is not penetrated, and bending the glass cover and the silicon on insulator substrate to remove the glass cover.

The invention can also provide a method for fabricating an avalanche photodiode, the method comprising the steps of:

processing a glass cover for protecting the surface of a FZ substrate;

etching with an alkaline agent a portion of a CZ substrate where a silicon nitride film of the CZ substrate is removed followed by suspending the progress of etching with a silicon oxide film in an SOI substrate to form a diaphragm;

dicing a thin part of the glass cover to a depth such

that the glass cover is not penetrated from the side of the glass cover;

dicing a part located at a relative position with a dicing line processed on a dicing line from the side of the CZ substrate to a depth such that the CZ substrate is not penetrated; and

bending the glass cover and the SOI substrate to remove the glass cover.

Further, the present invention provides a method for fabricating an avalanche photodiode comprising the steps of:

- (a) forming a metal thin film on a side of a glass substrate side, coating a photoresist, and patterning the photoresist;
- (b) etching said metal thin film in accordance with said patterned photoresist and etching the glass substrate with a fluoric acid agent by using the metal thin film as a mask;
- (c) removing the metal thin film and the photoresist used as the mask;
- (d) forming a metal thin film on the surface of the glass substrate, coating a photoresist, and patterning the photoresist;
- (e) etching the metal thin film in accordance with the patterned photoresist and etching the glass substrate with a fluoric acid agent by using the patterned metal thin film as a mask;
- (f) removing the metal thin film and the photoresist used as the mask;
- (g) forming a metal thin film by the sputtering process and vapour deposition, which constitutes an electrode on the side of the glass substrate, on the surface of the substrate which is etched, etching and patterning the metal thin film with photolithography technique; and
- (h) positioning and joining by contacting each other the electrode on the floating zone substrate of the silicon on insulator substrate with the electrode formed on the glass substrate.

Further, the method according to the present invention comprises:

forming a metal thin film on a side of a glass substrate and coating a photoresist to pattern the metal thin film;

etching a glass substrate with a fluorine agent;

removing a metal thin film and a photoresist used as a mask;

patterning a photoresist on the surface of the glass substrate;

etching the metal thin film in accordance with the patterned photoresist;

etching the glass substrate with a fluorine agent;

removing the metal thin film and the photoresist;

forming a metal thin film on the surface of the glass substrate that has been etched and processed followed by patterning the metal thin film;

positioning and joining by contacting each other an electrode on the FZ substrate of the SOI substrate with an electrode formed on a glass substrate for forming a junction.

The first substrate, or a part of the silicon on insulator substrate, can be a Czochralski (CZ) substrate.

In an avalanche photodiode thus constructed, the physical strength is strong even when the FZ substrate is thinned down, and at the same time, the scattering area of the incident light can be thinned down. Further, a deformation of the substrate during heat treatment (warp in the wafer) and the generation of the dislocation slip are reduced. Further, in a structure in which part of the first substrate is removed, electron beams or the like can be incident on this part. Further, when the avalanche photodiode is packaged in an IC package, the substrate on which a PN junction is formed is not directly joined with the IC package with the result that the photodiode is not affected by the heat accumulated in the IC package resulting from a rise in the peripheral temperature.

Further, in a method for fabricating an avalanche photodiode, since a step of forming a glass cover having a depression is included for protecting an element of the surface of a silicon substrate, the surface of the element is no longer etched with an alkaline agent. Further, an electrode is preliminarily formed on the glass substrate, and the electrode on the glass substrate and the electrode of the avalanche photodiode are positioned so as to contact each other, followed by joining the glass substrate and the SOI substrate with the result that a reverse bias can be applied to the PN junction which is formed on the FZ substrate by applying a voltage to an electrode on the glass substrate.

These and other objects, advantages, features, and uses will become more apparent as the description proceeds, when considered with the accompanying drawings.

Embodiments of the present invention will be explained hereinafter by way of example only with reference to the accompanying diagrammatic figures.

In order to more fully understand the drawings used in the detailed description of the present invention, a brief description of each drawing is provided.

Fig. 1 is a schematic sectional view showing an avalanche photodiode according to a first embodiment of the present invention;

Fig. 2 is a schematic sectional view showing an avalanche photodiode according to a second embodiment of the present invention;

Fig. 3 is a schematic sectional view showing an avalanche photodiode according to a third embodiment of the present invention;

Fig. 4 is a schematic sectional view showing an avalanche photodiode according to a fourth embodiment of the present invention;

Fig. 5 is a schematic sectional view showing an avalanche photodiode according to a fifth embodiment of the present invention;

Fig. 6 is a schematic sectional view showing an avalanche photodiode according to a sixth embodiment of the present invention;

Fig. 7 is a schematic sectional view showing an avalanche photodiode according to a seventh embodiment of the present invention;

Fig. 8 is a schematic sectional view showing an avalanche photodiode according to an eighth embodiment of the present invention;

Fig. 9 is a schematic sectional view showing an avalanche photodiode according to a ninth embodiment of the present invention;

Fig. 10 is a schematic sectional view showing an avalanche photodiode according to a tenth embodiment of the present invention;

Fig. 11 is a schematic sectional view showing an avalanche photodiode according to an eleventh embodiment of the present invention;

Fig. 12 is a schematic sectional view showing an avalanche photodiode according to a twelfth embodiment of the present invention;

Fig. 13 is a schematic sectional view showing an avalanche photodiode according to a thirteenth embodiment of the present invention;

Fig. 14 is a schematic sectional view showing an avalanche photodiode according to a fourteenth embodiment of the present invention;

Fig. 15 is a schematic sectional view showing an avalanche photodiode according to a fifteenth embodiment of the present invention;

Fig. 16 is a schematic sectional view showing an avalanche photodiode according to a sixteenth embodiment of the present invention;

Fig. 17 is a schematic sectional view showing an avalanche photodiode according to a seventeenth

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embodiment of the present invention, the view showing the embodiment before being packaged in an IC package;

Fig. 18 is a schematic top plan view seen from the direction of A of Fig. 17, the view showing the avalanche photodiode according to the seventeenth embodiment of the present invention;

Fig. 19 is a schematic bottom plan view seen from the direction of B of Fig. 17, the view showing the avalanche photodiode according to the seventeenth embodiment of the present invention;

Fig. 20 is a schematic sectional view showing a conventional avalanche photodiode;

Fig. 21 is a schematic sectional view showing the conventional avalanche photodiode of Fig. 20;

Fig. 22 is a schematic sectional view showing another conventional avalanche photodiode;

Fig. 23 is a schematic sectional view showing the conventional avalanche photodiode of Fig. 22;

Fig. 24A-24I are sectional views showing a first method for fabricating the avalanche photodiode according to the present invention; and

Fig. 25A-25K are sectional views showing a second method for fabricating the avalanche photodiode according to the present invention;

Fig. 1 is schematic sectional view of an avalanche photodiode according to a first embodiment of the present invention. For example, between a first substrate (hereinafter referred to as a substrate 1) comprising silicon and a second substrate 2 (hereinafter referred to as a floating zone (FZ) substrate 2) comprising a P-type silicon having a specific resistance of  $50 \Omega \cdot \text{cm}$  or more, an insulating film 5 comprising  $\text{SiO}_2$  which is formed by thermal oxidation or chemical vapour deposition (CVD) is formed. The insulating film 5 can be formed on the first substrate 1 and the FZ substrate 2 can be crystal grown on the insulating film 5. Thus, the substrate 1, FZ substrate 2 and insulating film 5 form a silicon on insulator (SOI) substrate. On the surface of the FZ substrate 2 on the opposite side from the substrate 1, for example, an N-type layer 16 doped with arsenic or phosphorus, and an N-type layer 17 contacting and surrounding the N-type layer 16 and doped with, for example, phosphorus, and a P<sup>+</sup>-type layer 18 doped with, for example, boron also surrounding the N-type layer 16 without contacting the N-type layer 17 are formed. Beneath the N-type layer 16, a P<sup>±</sup>-type layer 19 is formed in contact with the N-type layer 16. On the upper surface of the FZ substrate 2, an insulating film 7 comprising  $\text{SiO}_2$  formed by, for ex-

ample, thermal oxidation is formed. On the surface of the FZ substrate 2 on the side facing the substrate 1, a P<sup>+</sup>-type layer 24 doped with, for example, boron is formed.

On the insulating film 7, electrodes 3a and 3b, which are electrodes of the N-type layer 17 and the P<sup>+</sup>-type layer 18, are formed.

Since the substrate 1 has the effect of reinforcing the FZ substrate in the fabrication step thereof, a silicon substrate having the same thermal expansion coefficient is desirable. Considering the high temperature treatment process in a high temperature fabrication step, a silicon substrate 1 comprising a silicon CZ substrate which has crystal grown by the Czochralski Method and which endures heat treatment is the most desirable. Further, the FZ substrate needs a thickness of at least 100  $\mu\text{m}$ , and desirably 200  $\mu\text{m}$  or more.

When the structure of the embodiment of the invention is adopted in the avalanche photodiode, the specific resistance of the FZ substrate can be set to several  $\text{k}\Omega \cdot \text{cm}$  or more that cannot be obtained in the epitaxial layer of the prior art. Further, with the structure of the embodiment of the invention, the P<sup>+</sup>-type layer 24 can easily be formed to a thickness of 1  $\mu\text{m}$  or less as compared with a case of using an epitaxial layer wherein the thickness of the P<sup>+</sup>-type layer cannot be thinned down to several  $\mu\text{m}$  or less even by polishing. This improves the time resolution of the avalanche photodiode.

When the thickness of the FZ substrate in the conventional avalanche photodiode is 100  $\mu\text{m}$  or less, the deterioration problem occurs in device characteristics such as a reduction in the fabrication yield ratio and an increase in reverse bias leak current due to cracks of the substrate and an increase in the dislocation slips in thermal treatment and other fabrication steps. Further, when the FZ substrate has a thickness of 10  $\mu\text{m}$  or less, the efficiency of X-ray detection is not practical. Consequently, the effect of the present embodiment is large when the FZ substrate has a thickness of from 10  $\mu\text{m}$  to 100  $\mu\text{m}$ .

Fig. 2 is a schematic sectional view of an avalanche photodiode according to a second embodiment of the present invention. In the second embodiment, part of the substrate 1 in the first embodiment is removed, and a substrate opening 14 is provided. At least in a part of a portion immediately beneath the PN-junction located at a position where the N-type layer 16 and the P<sup>±</sup>-type layer 19 in the FZ substrate 2 contact each other, the opening 14 is provided. In the opening 14, the insulating film 5 is removed, too. The other aspect of the second embodiment is the same as the first embodiment.

When a radiation or the like is allowed to be incident from the opening 14 or when the avalanche photodiodes in the second embodiment are used with being stacked, the insulating film 5 is desirably removed as shown in Fig. 2. When visible rays or the like are permitted to be incident from the opening 14, the insulating film 5 may be present without any problem when the insulating film

5 is formed of an oxide film having a thickness of 150 nm or less. Further, when electron beams, light or the like are allowed to be incident from the opening 14, it is more desirable that the opening 14 is smaller than P<sup>±</sup>-type layer 19 as the amplification area. Because the non-uniformity in the amplification rate depending on the incident position can be small.

In the case where the radiation or the like is allowed to be incident from the side of the N-type layer 16, the amplification rate becomes non-uniform or lowered when the depth to which the incident radiation or the like is allowed to infiltrate into silicon is located in the vicinity of the P<sup>±</sup>-type layer 19 which constitutes an amplification area. However, when the avalanche photodiode of the second embodiment is used to allow such radiation to be incident from the opening 14, such a problem is not generated. Consequently, in the second embodiment, when the radiation or the like is allowed to be incident from the opening 14, more favourable characteristics can be obtained. Further, it is more significant to improve the detection efficiency by forming the P<sup>±</sup>-type layer 19 to 1 μm or less.

In the second embodiment, when a silicon surface direction (100) substrate is used as the substrate 1, a large stress concentrated on the edge of the opening 14 can be alleviated because the opening 14 intersects at an obtuse angle with a wall part in the (111) direction where the substrate 1 is removed by anisotropic etching using a potassium hydroxide solution.

Fig. 3 is a schematic sectional view showing the avalanche photodiode according to a third embodiment of the present invention. The electrode 3b, contacts the P<sup>+</sup>-type layer 18 in the above-mentioned second embodiment. But in the third embodiment, this is formed so that the electrode 3b contacts the P<sup>+</sup>-layer 24 of the FZ substrate 2 on the side of the substrate 1. Further, between the electrode 3b and the substrate 1, an insulating film 25 comprising an oxide film is formed.

When electron beams, light or the like are allowed to be incident from the opening 14, the photodiode having the opening 14 smaller than the P<sup>±</sup>-type layer 19 which constitutes an amplification area is desirable because the non-uniformity in the amplification rate depending on the incident position becomes small the same as described for the second embodiment. In the third embodiment, since the size and shape of the opening 14 can be determined according to the electrode 3b having one percent thickness compared with that of more than 100 μm of the substrate 1, the precision of the shape can be increased and the manufacturing size thereof can be made to a smaller size of margin. The other aspect of the third embodiment is the same as the first embodiment.

By adopting the structure of the third embodiment, the series resistance between electrodes can be reduced. Therefore, an avalanche photodiode having an excellent time resolution of a signal can be obtained.

Fig. 4 is a schematic sectional view of the avalanche

photodiode according to a fourth embodiment of the present invention. An insulating film 5 is formed between the substrate 1 and the FZ substrate 2. On the surface of the FZ substrate 2 on the side facing the substrate 1, for example, an N-type layer 16 doped with arsenic or phosphorus, an N-type layer 17 doped with, for example, phosphorous contacting and surrounding the N-type layer 16 and a P-type layer 18 doped with, for example, boron and surrounding the N-type layer 17 without contacting the N-type layer 17 are formed. On the lower part of the N-type layer 16, a P<sup>±</sup>-type layer 19 doped with boron is formed in contact with the N-type layer 16. On the surface of the FZ substrate 2 on the opposite side from the substrate 1, a P<sup>+</sup>-type layer 24 doped with, for example, boron and an electrode 3b thereof are formed. Further, between the electrode 3a and the substrate 1, an insulating film 26 comprising an oxide film is formed.

The fourth embodiment has a structure in which the FZ substrate 2 of the second embodiment is turned up-side-down with respect to the substrate 1. While the radiation or the like is preferably allowed to be incident from the side of the P<sup>+</sup>-type layer 24 located opposite to the P<sup>±</sup>-type layer 19 which constitutes the amplification area for the measurement of a radiation or the like having a relatively small infiltration depth into the silicon, providing the P<sup>+</sup>-type layer 24 at a remote position from the substrate 1 as in this embodiment allows measurement with the P-type layer closer to the radiation source or the like because the substrate 1 is absent on the incident side. If the substrate 1 was not absent, it would hinder the approach of incident radiation.

Fig. 5 is a sectional view of the avalanche photodiode according to a fifth embodiment of the present invention. In this embodiment, the substrate 1 having no avalanche photodiode formed thereon and a glass substrate 4 are joined to further improve the mechanical strength of the FZ substrate 2 which is joined with the substrate 1. In joining the substrate 1 with the glass substrate 4, a voltage of 200 to 400 V is applied while heating both substrates at 400 to 500°C for joining the substrates by the anodic bonding process. When the anodic bonding process is used like the present case, no adhesive layer exists so that no degassing can be performed and the measurement can be made even in vacuum. As other kinds of the junction method, the junction using the low melting point glass can be made possible.

Fig. 6 is a sectional view of the avalanche photodiode according to a sixth embodiment of the present invention. In this embodiment, through holes 6 and 9 are formed in one part of a glass substrate 4, which is positioned at a linear relation with the PN junction formed in the FZ substrate 2, and in one part of the integrated circuit (IC) package 8 respectively. These through holes 6 and 9 are required when X-rays or the like are to be detected. In the structure in which no through hole is formed as shown in Fig. 5, no problems arise with general light. However, when the X-ray is to be detected, problem arises. After the X-ray incident from the FZ substrate 2 pass-

es through the substrate 1, the X-ray collides with the glass substrate 4 and is scattered to return to the substrate 1 again. That is detected as a noise. Further, by forming a through hole as shown in Fig. 6, light can be incident from the side of the IC package.

Fig. 7 is a sectional view of the avalanche photodiode according to a seventh embodiment of the present invention. In this embodiment, the electrodes 3a and 3b for applying a voltage to the PN junction are opposed to and are contacted to the electrodes 11 formed on the glass substrate 4 for electric conduction. Therefore, each electrode 11 on the glass substrate is connected to a lead pin 10 of the IC package 8 so that a voltage can be applied to the PN junction by applying a voltage to the lead pins.

Fig. 8 shows the avalanche photodiode according to an eighth embodiment of the present invention wherein through holes 6 and 9 are formed in the glass substrate 4 and the IC package 8 respectively according to the seventh embodiment as shown in Fig. 7. The effect of the present invention is that the invention can be used for the detection of the X-ray or the like as described above.

Fig. 9 shows the avalanche photodiode according to a ninth embodiment of the present invention wherein the substrate 1 has a structure in which a portion immediately below the PN junction is removed. This means that a blind area is removed for forming only a feeling area. In this embodiment, there is shown an example in which such a method for forming a diaphragm is performed with anisotropic etching using an alkaline liquid such as sodium hydroxide solution or the like. With such a structure, the leak current generated by the energy incident on the blind area can be inhibited, thereby an avalanche photodiode having favourable response characteristics can be realised. In this manner, the PN junction is formed within the FZ substrate 2 and the thickness thereof is several tens of  $\mu\text{m}$ . Consequently, to reinforce the mechanical strength, the PN junction is joined with the glass substrate 4. Further, even when the PN junction is used under high temperature, the direct influence of heat accumulation on the IC package 8 is avoided. When this structure is adopted in the photodiode, it is necessary to widen electrodes 3a and 3b for applying a voltage to the PN junction even to an area where the substrate 1 remains. This is because there is a high possibility that diaphragm is destroyed when the electrode and the lead pin are connected with wire bonding or the like.

Fig. 10 shows an avalanche photodiode according to a tenth embodiment of the present invention wherein through holes 6 and 9 are formed on a glass substrate 4 and an IC package 8 respectively, having a structure as shown in Fig. 9. This is required when the X-ray or the like is incident on the photodiode. After the X-ray passes through the substrate 1, the X-ray collides with the glass substrate 4 with the result that the X-ray is scattered and noise is generated. Further, the X-ray can be incident from the side of the IC package 8. Further, it is possible to assume a structure to which an avalanche

photodiode is connected.

Fig. 11 is a schematic sectional view showing the avalanche photodiode according to an eleventh embodiment of the present invention. This type of photodiode takes an electric conduction by contacting electrodes 3a and 3b for applying a voltage to the PN junction formed in the FZ substrate 2 with the electrode 11 formed on the side of the glass substrate 4.

The FZ substrate 2 and the glass substrate 4 are joined to each other by the anodic bonding process, a process using the low melting point glass, or the like. Further, the glass substrate 4 which is joined with the FZ substrate 2 is joined with the IC package 8. The glass substrate 4 is joined with the IC package 8 by using an eutectic junction, a low melting point glass or a ceramic adhesive requiring no degassing. An electric connection is made to provide an electric conduction by connecting an electrode 11 on the glass substrate side and the lead pin 10 of the IC package 8 with a metal wire 15. By adopting such a structure, a light signal can be incident from the substrate 1. When light is incident from this direction, the depth of the infiltration of the radiant rays or the like into the substrate becomes distant from the layer which constitutes an amplification area so that it never happens that the amplification rate is distributed and lowered.

Fig. 12 is a schematic sectional view showing the avalanche photodiode according to a twelfth embodiment of the present invention. In the embodiment, in addition to the structure as shown in Fig. 11, through holes 6 and 9 are formed on the glass substrate 4 and the IC package 8, respectively. This is required for allowing the X-ray or the like to be incident on the photodiode. The X-ray collides with the glass substrate 4 and is scattered after passing through the FZ substrate 2 so that noise is generated. Further, the X-ray can be incident from the side of the IC package 8. Furthermore, it is possible to assume a structure for stacking the avalanche photodiode, because the provision of through holes 6 and 9 reduces the degree of X-ray decay in each avalanche photodiode.

Fig. 13 is a schematic sectional view showing the avalanche photodiode according to a thirteenth embodiment of the present invention. This embodiment is an example in which an avalanche photodiode as shown in Fig. 3 is packaged. The substrate 1 is joined with the glass substrate 4 and at the same time, the electrode 3b contacts the electrode 11 on the glass substrate 4 to provide an electric conduction. The electrode 3b is formed so as to contact the P+ type layer 24 on the side of the FZ substrate 2 facing the substrate 1. Further, between the electrode 3b and the substrate 1, for example, an insulating film 25 comprising an oxide film is formed. Consequently, the electrode 3a and the electrode 11 are connected to the lead pin 10 of the IC package 8, respectively, with a metal wire 15, or the like, with the result that voltage is applied to the PN junction if voltage is applied to the lead pin 10.

Fig. 14 is a schematic sectional view showing the

avalanche photodiode according to a fourteenth embodiment of the present invention. In this embodiment, in addition to the structure of the avalanche photodiode shown in Fig. 13, through holes 6 and 9 are formed in the glass substrate 4 and the IC package 8 respectively. This is required when the X-ray or the like is incident on the photodiode. After the X-ray passes through the substrate, the X-ray collides with the glass substrate 4 and is scattered with the result that noise is generated. Further, radiation from the side of the IC package 8 can also be incident. Furthermore, it is also possible to assume a structure for stacking the avalanche photodiode.

Fig. 15 shows the avalanche photodiode according to a fifteenth embodiment of the present invention. The embodiment is an example in which the avalanche photodiode shown in Fig. 4 is packaged.

Voltage is applied from the lead pin 10 to the PN junction by connecting the electrodes 3a and 3b thereto. In this structure, the mechanical strength is reinforced since the joint area between the FZ substrate 2 and the glass substrate 4 is increased.

Fig. 16 shows the avalanche photodiode according to a sixteenth embodiment of the present invention. In the glass substrate 4 and the IC package 8 shown in Fig. 15, this embodiment is that through holes 6 and 9 respectively are formed. The through holes 6 and 9 are required when the X-ray or the like is incident on the photodiode. After the X-ray passes through the FZ substrate 2, the X-ray collides with the glass substrate 4 and is scattered with the result that noise is generated. Further, radiation from the side of the IC package 8 can also be incident. And furthermore it is possible to assume a structure for stacking the avalanche photodiodes.

Fig. 17 is a schematic sectional view showing the avalanche photodiode according to a seventeenth embodiment of the present invention. Fig. 17 shows a state before the avalanche photodiode is packaged in the IC package, the view showing a state after the avalanche photodiode is joined with the glass substrate 4. Electrodes 3a and 3b for applying a voltage to the PN junction formed in the FZ substrate 2 contact electrodes 11 on the glass substrate 4. Further, on the glass substrate 4, projections 28 are formed in order to get good electric contact, so that electrodes 11 are formed on the projections 28.

Fig. 18 is a schematic top plan view obtained when Fig. 17 is seen from the direction A, the view showing the avalanche photodiode according to the seventeenth embodiment of the present invention. When the substrate 1 having surface direction (100) is subjected to anisotropic etching, (111) surface 29 appears. The silicon surface 23 is the surface of the P+-type layer 24 formed on the FZ substrate 2 as shown in Fig. 17. Further, on the glass substrate 4, electrodes 11 are formed.

Fig. 19 is a schematic bottom plan view obtained when Fig. 17 is seen from the direction B, the view showing the avalanche photodiode according to the seventeenth embodiment of the present invention. The elec-

trodes 11 on the glass substrate 4 contact electrodes 3a and 3b for applying a voltage to the PN junction. Consequently, the embodiment functions as an avalanche photodiode by applying a voltage to the electrodes on the glass substrate. Further, in the glass substrate 4, a through hole 6 is formed thereby preventing the X-ray from colliding with the glass substrate 4.

Figs. 24A-I show a method for fabricating the avalanche photodiode according to the present invention.

- 10 Figs. 24A-I are views showing a method for converting the avalanche photodiode shown in Fig. 1 into an avalanche photodiode (photodiode which is thinned having a sensing part thinned down by anisotropic etching) shown in Fig. 2. Out of the above-mentioned drawings, 15 Figs. 24A through 24E show steps for fabricating a glass cover 101a for protecting the surface which is not etched from an etching solution.

Fig. 24A shows a glass substrate 101 before processing.

- 20 Fig. 24B shows a state in which a metal thin film 102 is formed on the glass substrate 101.

Fig. 24C shows a state in which a photoresist 103 is formed on the metal thin film 102.

- 25 Fig. 24D shows a state in which the photoresist 103 on the metal thin film 102 and the metal thin film 102 are patterned by the photolithography technology.

- 30 Fig. 24E shows a step of etching the glass substrate 4 with fluoric acid agent by using the metal thin film 102 and the photoresist 103 obtained in the previous process as a mask. Further, although not shown in the drawings, the photoresist 103 and the metal thin film 102 are removed by etching to obtain a glass cover 101a having projections.

- 35 Fig. 24F shows a state in which the glass cover 101a which is formed by the previous step shown in Fig. 24E and the avalanche photodiode element 104 are laminated to each other. A method for laminating the glass cover 101a with the avalanche photodiode element 104 includes the anodic bonding process and the method using 40 the low melting point glass, the eutectic junction process, and the like. This step is for protecting the surface of the avalanche photodiode element from the agent used for etching a silicon substrate 106 at the following step shown in Fig. 24G.

- 45 Fig. 24G shows a step that a silicon nitride film 105 is used as a mask to subject the silicon substrate 106 to the anisotropic etching with an alkali agent such as potassium hydroxide or the like. It is also possible to subject the silicon substrate 106 to the isotropic etching with fluoric acid agent or the like. In the etching of the silicon substrate 106, the etching process is suspended at a silicon oxide 107 in the SOI substrate (a substrate in a structure in which the silicon semiconductor substrate is laminated by sandwiching an insulating film which is described as

- 50 the first means for solving the problem) which forms an avalanche photodiode element 104. Here, the silicon substrate 106 is taken out of the agent to be cleaned. Fig. 24G shows a state in which the silicon oxide film is

etched and removed with fluoric acid agent after that.

Fig. 24H shows a state in which the silicon substrate has been diced from the glass cover 101a and the avalanche photodiode element 104. At this time, when the glass cover 101a and the avalanche photodiode element 104 are diced at the same time, cooling water at the time of dicing may trap the dicing powders which adhere to the surface of the avalanche photodiode element 104 and cannot be removed. Consequently, the dicing is suspended at the depth shown with the dicing line 111 shown in Fig. 24H so that both the silicon substrate and the glass cover 101a are not completely diced off.

Fig. 24I shows a state in which the substrate is bent along the dicing line 111 used at the step shown in Fig. 24H so that the avalanche photodiode element 104 is completed by removing the glass cover 101a on the surface and separating the glass cover 101a on the surface from the wafer of the avalanche photodiode element 104.

Figs. 25A-25K show a method for fabricating a glass substrate used in an embodiment shown in Fig. 17 or the like. The steps are intended to join an avalanche photodiode element 104 with a glass substrate 4 on which an electrode is formed to obtain a function as an avalanche photodiode by applying a reverse bias to the electrode on the glass substrate side.

Fig. 25A shows a glass substrate 4 before processing.

Fig. 25B shows a state in which a through hole 6 is formed in the glass substrate by ultrasonic wave or the like. This through hole 6 is formed for preventing X-ray or the like from being scattered or reflected by the glass substrate when the X-ray or the like are incident on the avalanche photodiode element.

Fig. 25C shows a state in which the metal thin film 102 and the photoresist 103 are formed on the glass substrate 4 and patterned for etch processing the glass substrate 4.

Fig. 25D shows a state in which the glass substrate 4 is etched in accordance with the metal thin film 102 and the photoresist 103 which are formed at the step shown in Fig. 25C.

Fig. 25E shows a state after the glass substrate has been etched. In Fig. 25E, projection 108 is a part which is joined with the avalanche photodiode element in a following step.

Fig. 25F shows a state in which a metal thin film 102 and a photoresist 103 are formed on the glass substrate 4 for the second glass etching.

Fig. 25G shows a state in which the metal thin film 102 and the photoresist 103 which are formed at the preceding step are patterned.

Fig. 25H shows a state in which the glass substrate is etched in accordance with the metal thin film 102 and the photoresist 103 formed at the step shown in Fig. 25G.

Fig. 25I shows a state after the second etching of the glass substrate. The projection 109 formed at this step is a portion where an electrical connection is formed in contact with the avalanche photodiode element in a

following step.

Fig. 25J is a state in which the metal thin film 110 formed of aluminium or the like is formed and patterned, which constitutes an electrode material on the glass side.

Fig. 25K shows a state in which the glass substrate and the avalanche photodiode which have been completed up to the step shown in Fig. 25J are joined. The joining method may include the anodic bonding process and the method using the low melting glass or the like.

As described above, an avalanche photodiode according to the present invention is provided on a FZ-SOI substrate and part of the substrate 1 is removed to expose the FZ substrate so that a shallow depletion layer is formed on the surface thereof. Consequently, an avalanche photodiode can be formed which has a very high sensitivity and a high time resolution. Further, these avalanche photodiode element which can be joined with glass substrate can be packaged in various ways. Therefore, the effect of the present invention is that the mechanical strength can be increased so that the warp and the deformation of the substrate can be prevented.

The avalanche photodiode of the present invention can be used even in vacuum because of the absence of degassing when the substrate and the glass substrate are joined by anodic bonding process or the method using the low melting point glass. Further, by forming the through hole in the glass substrate and the IC package, not only the light detection, but also the X-rays or the like can be detected.

An avalanche photodiode according to the present invention comprises a first insulating film formed on a first substrate;

a second substrate comprising a floating zone silicon semiconductor substrate which is crystal grown on said first insulating film;

a PN-junction formed on said second substrate; a plurality of electrodes for applying a voltage to said PN-junction which is formed on said second substrate by sandwiching a second insulating film therebetween;

wherein said first substrate is joined with a glass substrate, the surface of the first substrate is joined with an integrated circuit package, and said plurality of electrodes are electrically connected with a lead pin of the integrated circuit package.

An avalanche photodiode according to the present invention comprising a PN-junction formed on a second substrate;

a plurality of electrodes for applying a voltage to said PN-junction which are formed on a surface of said second substrate by sandwiching a second insulating film; wherein the surface of said second substrate on which said plurality of electrodes are formed is joined with the surface of a glass substrate on which a second electrode is formed, said plurality of electrodes on the glass substrate are electrically conducted to each other, the surface of the glass substrate opposite to the surface where the second electrode is formed is joined with an

integrated circuit package, and said second electrode formed on the glass substrate is electrically connected to the lead pin of the integrated circuit package.

The foregoing description has been given by way of example only and it will be appreciated by a person skilled in the art that modifications can be made without departing from the scope of the present invention.

### Claims

1. An avalanche photodiode comprising:
  - a first insulating film (5) formed on a first substrate (1);
  - a second substrate (2) comprising a floating zone silicon semiconductor substrate which is crystal grown on said first insulating film;
  - a PN-junction formed on said second substrate;
  - a plurality of electrodes (3a, 3b) for applying a voltage to said PN-junction which is formed on said second substrate;
  - wherein said first substrate is joined with a glass substrate (4), the surface of the glass substrate is joined with an integrated circuit package (8), and said plurality of electrodes are electrically connected with a lead pin (10) of the integrated circuit package.
2. An avalanche photodiode according to claim 1 wherein said first substrate is removed at least at one part of the portion (14) located immediately below the PN junction in said second substrate.
3. An avalanche photodiode according to claim 2 wherein said first substrate is a silicon semiconductor substrate having a (100) surface direction.
4. An avalanche photodiode according to claim 2 wherein an impurity is selectively doped into the surface of the second substrate where said first substrate is removed.
5. An avalanche photodiode comprising:
  - a PN-junction formed on a second substrate (2);
  - a plurality of electrodes (3a, 3b) for applying a voltage to said PN-junction; wherein the surface of said second substrate on which said plurality of electrodes are formed is joined with the surface of a glass substrate (4) on which a second electrode (11) is formed, said plurality of electrodes and said second electrode on the glass substrate are electrically connected to each other, the surface of the glass substrate opposite to the surface where the second electrode is formed is joined with an integrated circuit package (8), and said second electrode formed on the glass substrate is electrically connected to the

lead pin (10) of the integrated circuit package.

6. An avalanche photodiode according to claim 1 or 5 wherein a through hole (6) is formed in a portion of said glass substrate immediately below the part where PN-junction is formed in the second substrate, and a through hole (9) is formed in the integrated circuit package located at the position which linearly connects said through hole with said part where the PN junction is formed.
7. An avalanche photodiode according to claim 6 wherein said first substrate is removed at least in one part immediately below the PN-junction in said second substrate.
8. An avalanche photodiode according to claim 7 wherein an impurity is selectively doped only into the surface of the part of said second substrate where said first substrate is removed, a third electrode is formed on the surface of said first substrate which is not joined with said second substrate to electrically connect with a region where said impurity is doped, a voltage is applied to the PN junction from a first electrode formed on the surface of the second substrate, the second electrode formed on the glass substrate and said first electrode contact each other to be electrically connected, and said second electrode formed on said glass substrate and the third electrode formed on said first substrate, are each electrically connected to a lead pin of the integrated circuit package.
9. A method for fabricating an avalanche photodiode comprising the steps of:
  - (a) forming a metal thin film (102) on one side of a glass substrate (101);
  - (b) patterning said metal thin film;
  - (c) etching said metal thin film by using a patterned photoresist (103) as a mask;
  - (d) etching said glass substrate with a fluoric acid agent by using said metal thin film as the mask; and
  - (e) removing the photoresist and the metal thin film used as a mask, and processing a glass cover (101a) for protecting the surface of a floating zone substrate (104);
  - (f) protecting the floating zone substrate by opposing an etched surface of said glass cover to a floating zone substrate of a silicon on insulator substrate on which the avalanche photodiode is formed to join the floating zone substrate

with a portion of the glass cover where the metal thin film is removed;

(g) forming a diaphragm by etching with an alkaline agent a portion of the silicon on insulator substrate where a silicon nitride film (105) is removed to terminate the progress of etching with a silicon oxide film in the silicon on insulator substrate;

(h) dicing a thin portion of the etched portion of the glass substrate from the side of the glass substrate to a depth such that the glass substrate is not penetrated; and

(i) dicing a portion of the silicon on insulator substrate located at a relative position with the dicing line which is processed on said glass substrate to a depth such that the silicon on insulator substrate is not penetrated, and bending the glass cover and the silicon on insulator substrate to remove the glass cover.

**10. A method for fabricating an avalanche photodiode comprising the steps of:**

(a) forming a metal thin film (102) on a side of a glass substrate (4), coating a photoresist (103), and patterning the photoresist;

(b) etching said metal thin film in accordance with said patterned photoresist and etching the glass substrate with a fluoric acid agent by using the metal thin film as a mask;

(c) removing the metal thin film and the photoresist used as the mask;

(d) forming a metal thin film (102) on the surface of the glass substrate, coating a photoresist (103), and patterning the photoresist;

(e) etching the metal thin film in accordance with the patterned photoresist and etching the glass substrate with a fluoric acid agent by using the patterned metal thin film as a mask;

(f) removing the metal thin film and the photoresist used as the mask;

(g) forming a metal thin film (110) by the sputtering process and vapour deposition, which constitutes an electrode on the side of the glass substrate, on the surface of the substrate which is etched, etching and patterning the metal thin film with photolithography technique; and

(h) positioning and joining by contacting each

other the electrode on the floating zone substrate (104) of the silicon on insulator substrate with the electrode formed on the glass substrate.

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FIG. 1

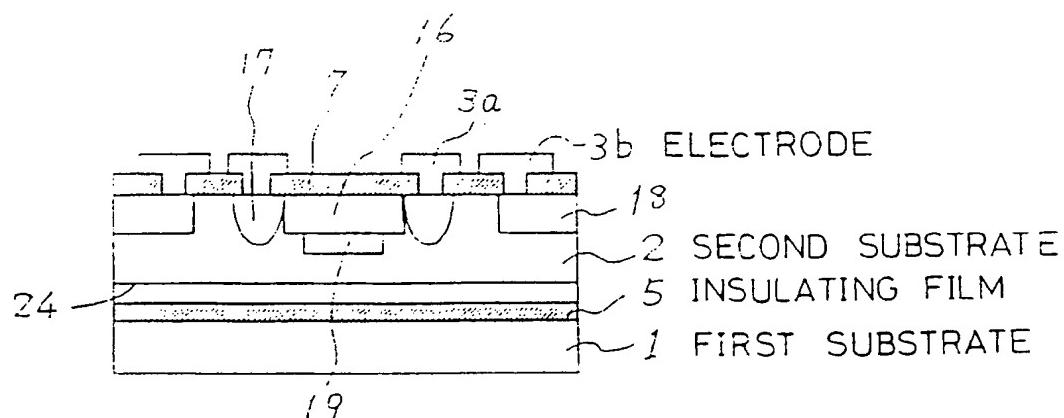


FIG. 2

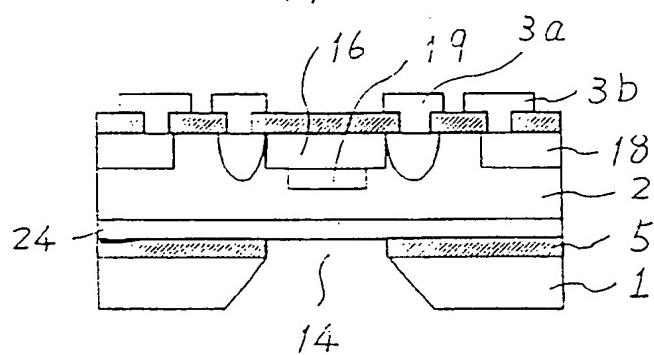


FIG. 3

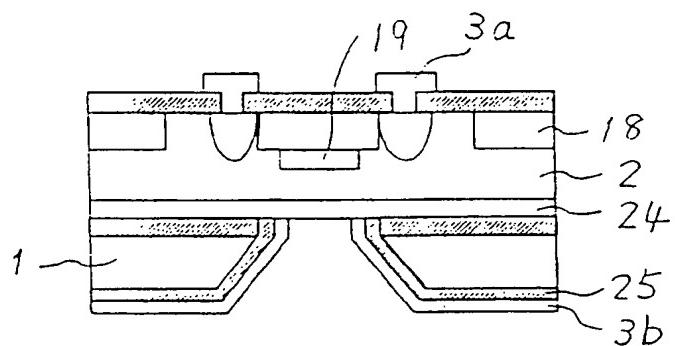


FIG. 4

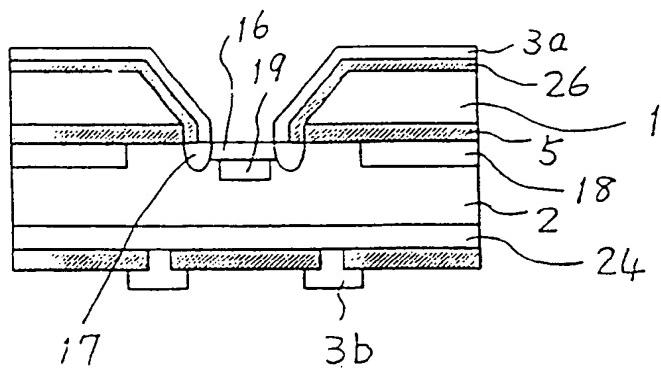


FIG. 5

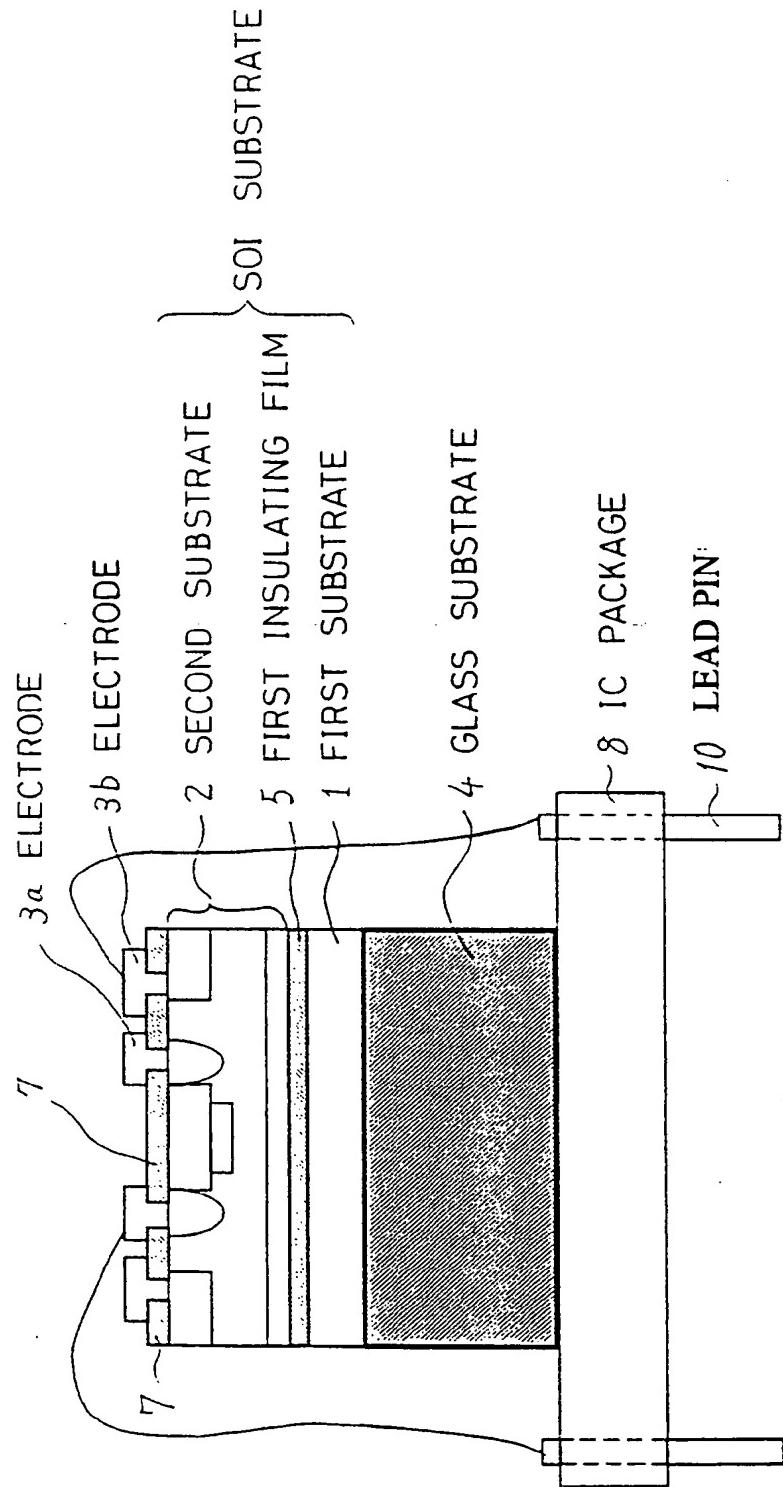


FIG. 6

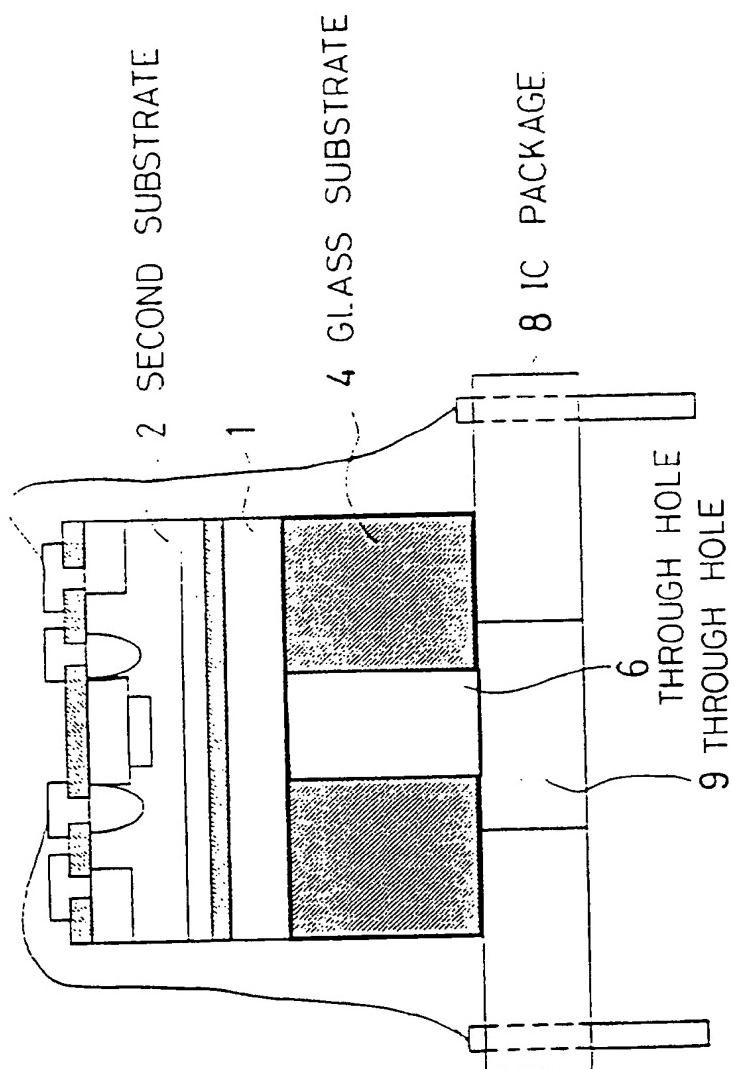


FIG. 7

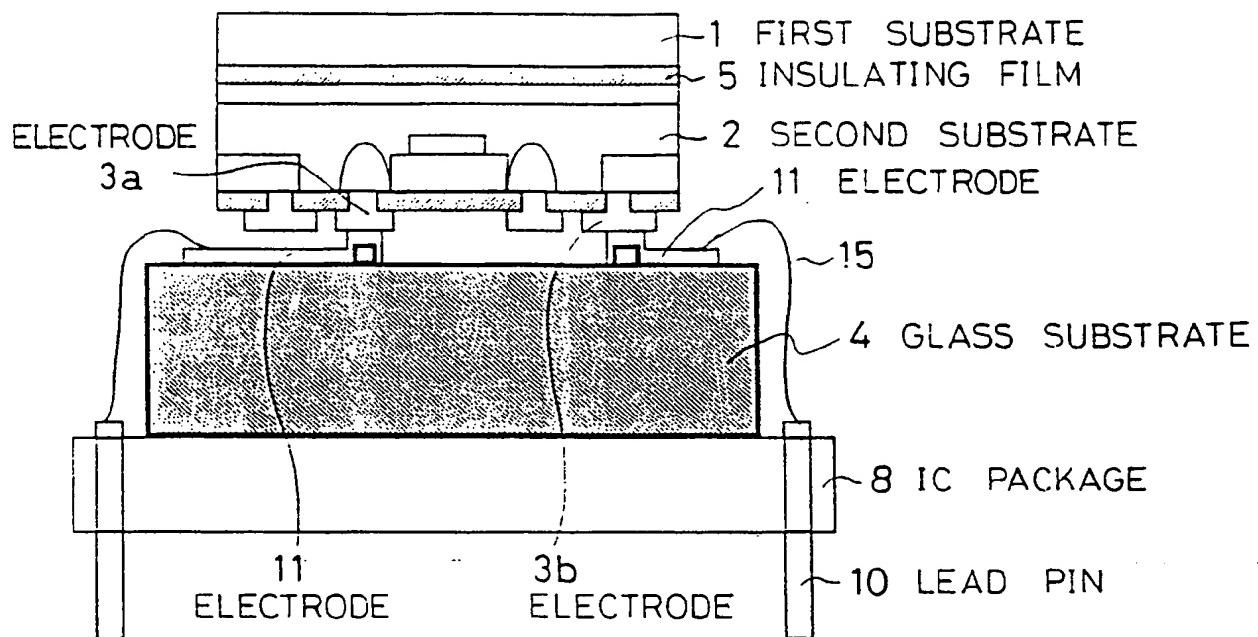


FIG. 8

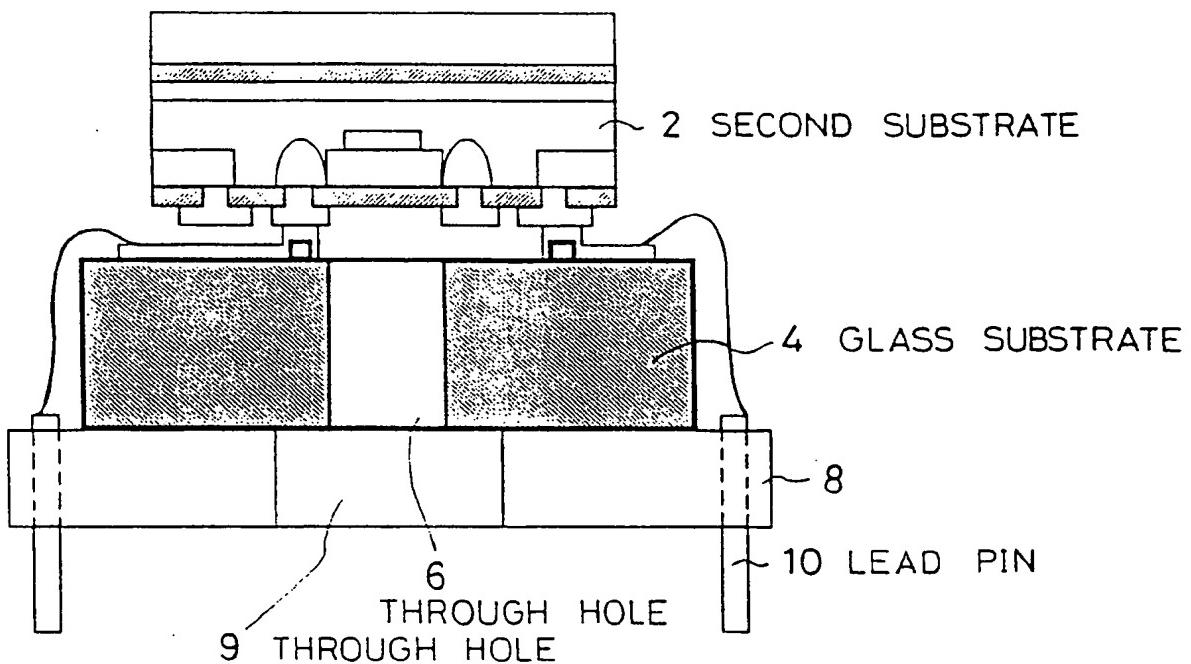


FIG. 9

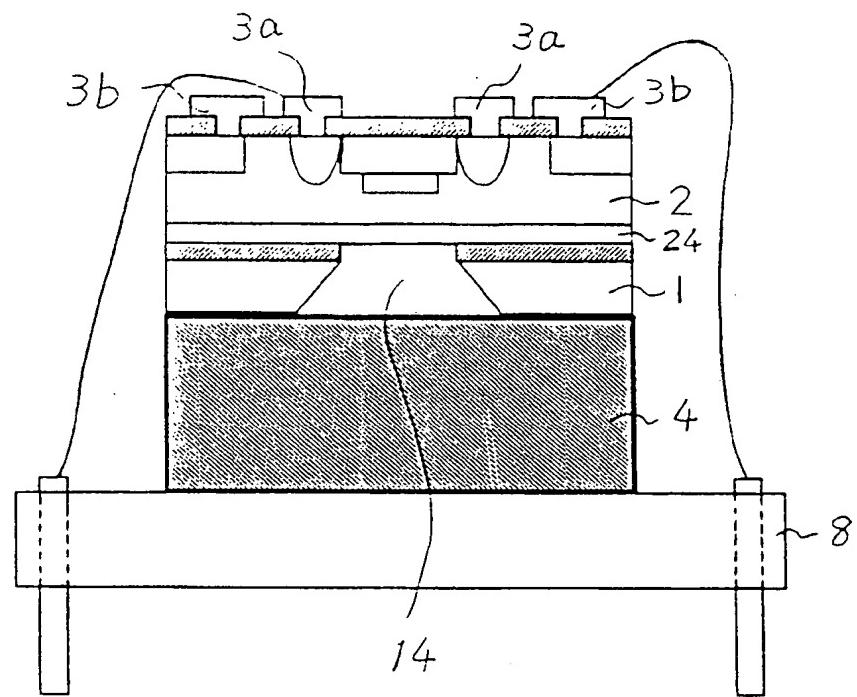


FIG. 10

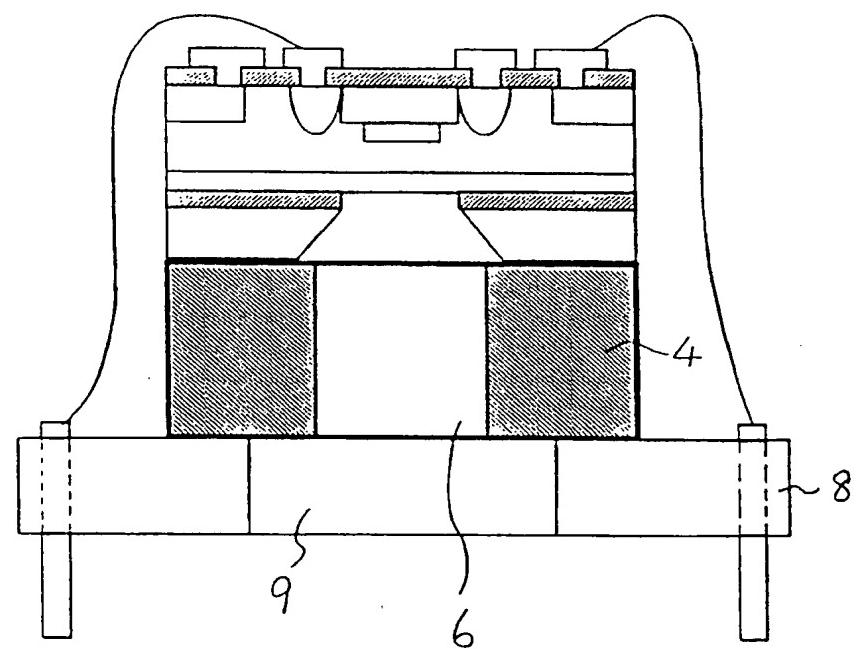


FIG. II

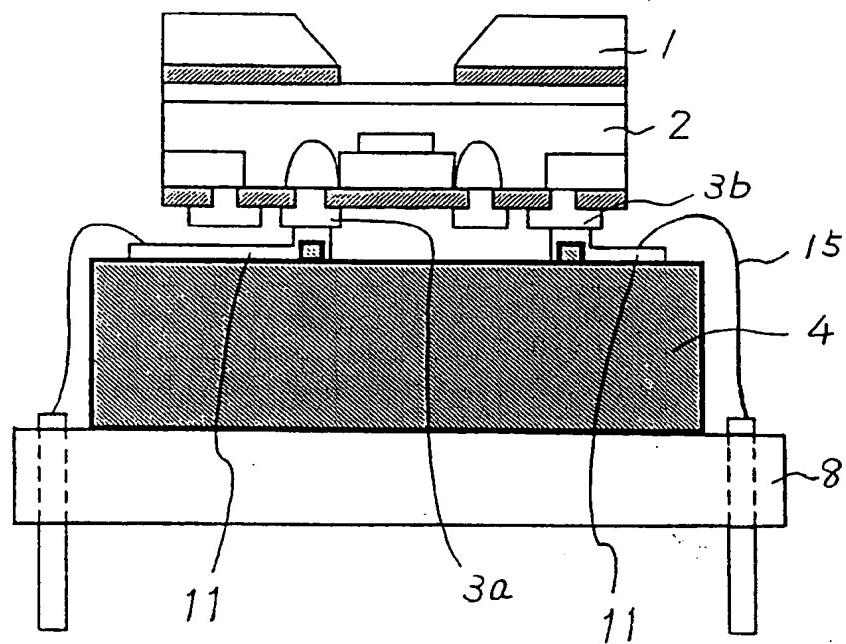


FIG. 12

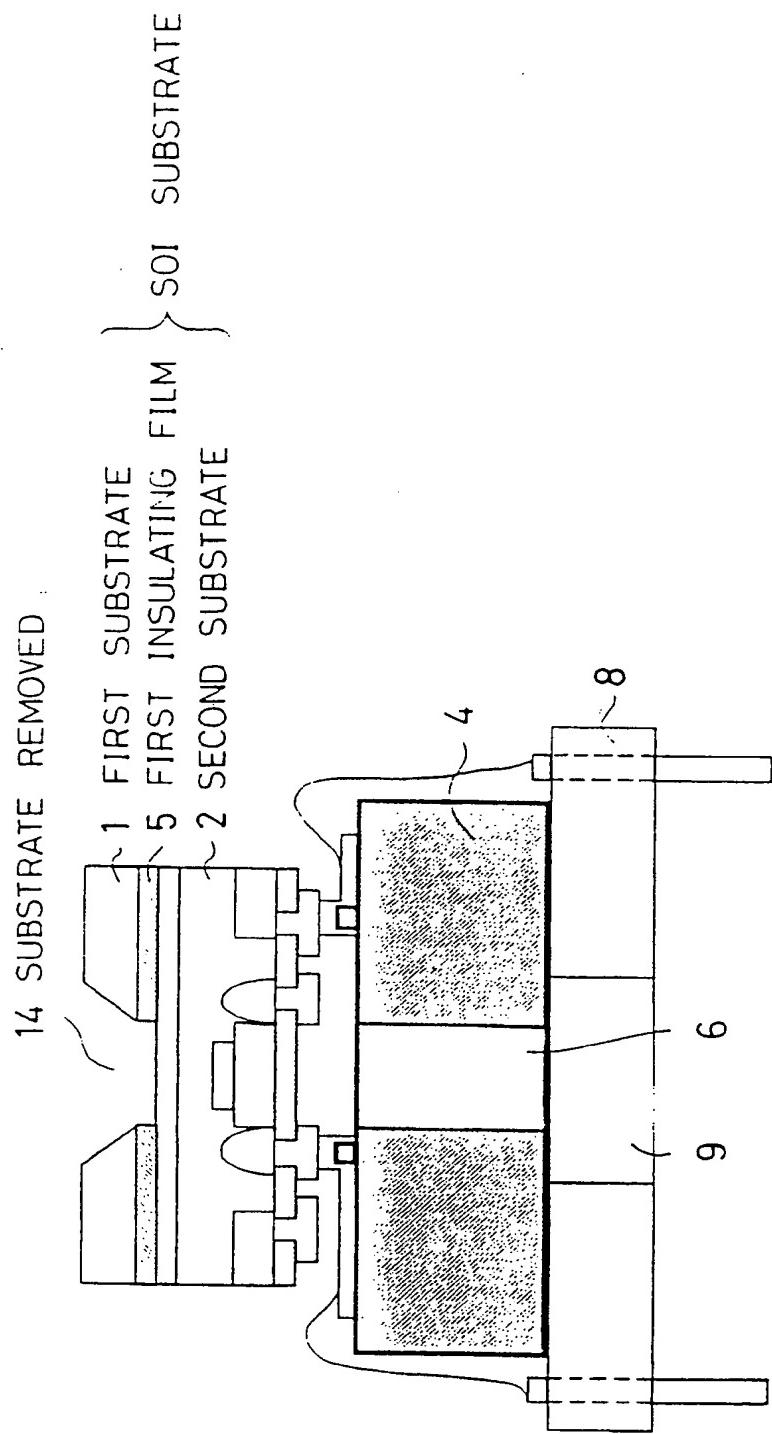


FIG. 13

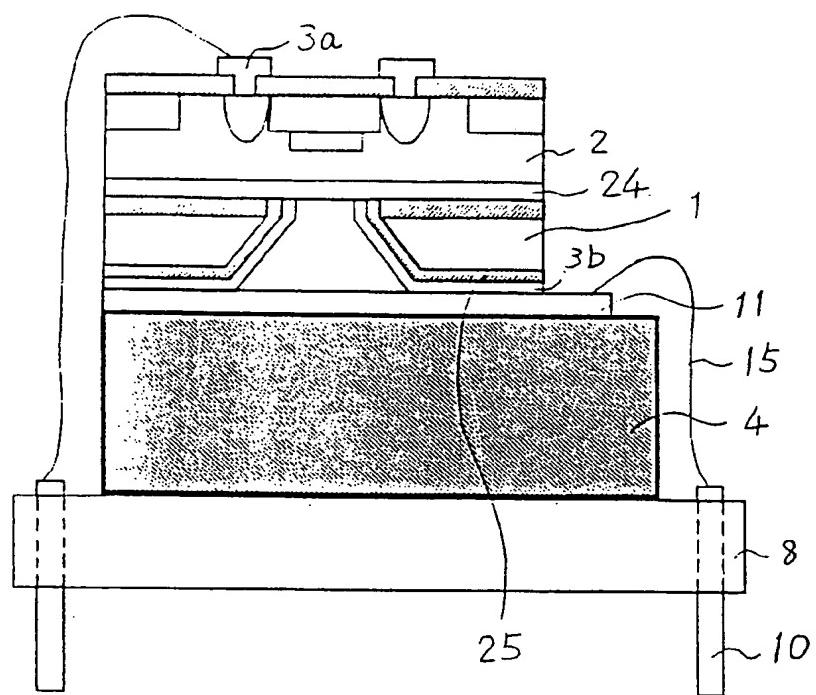


FIG. 14

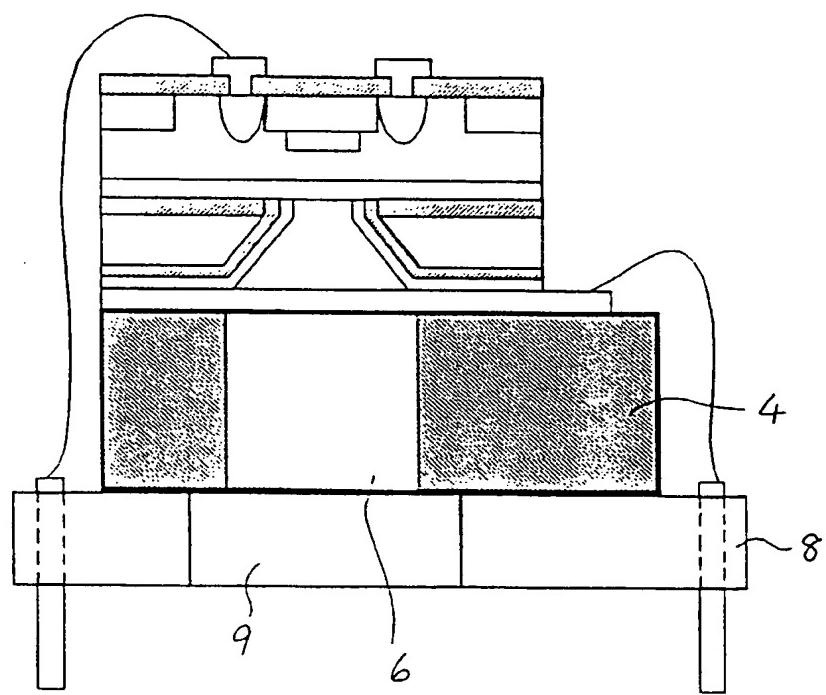


FIG. 15

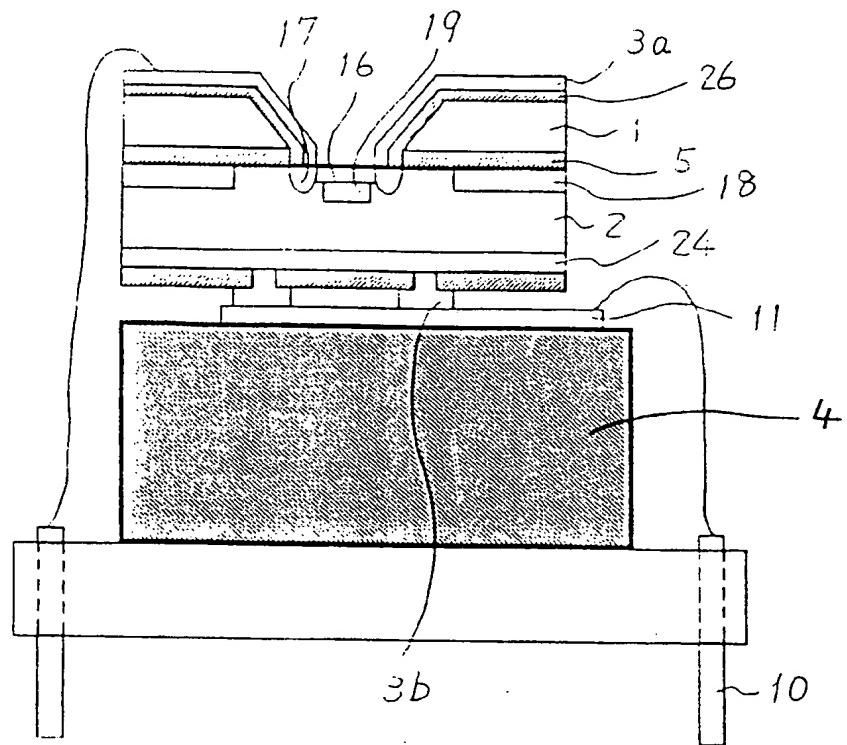


FIG. 16

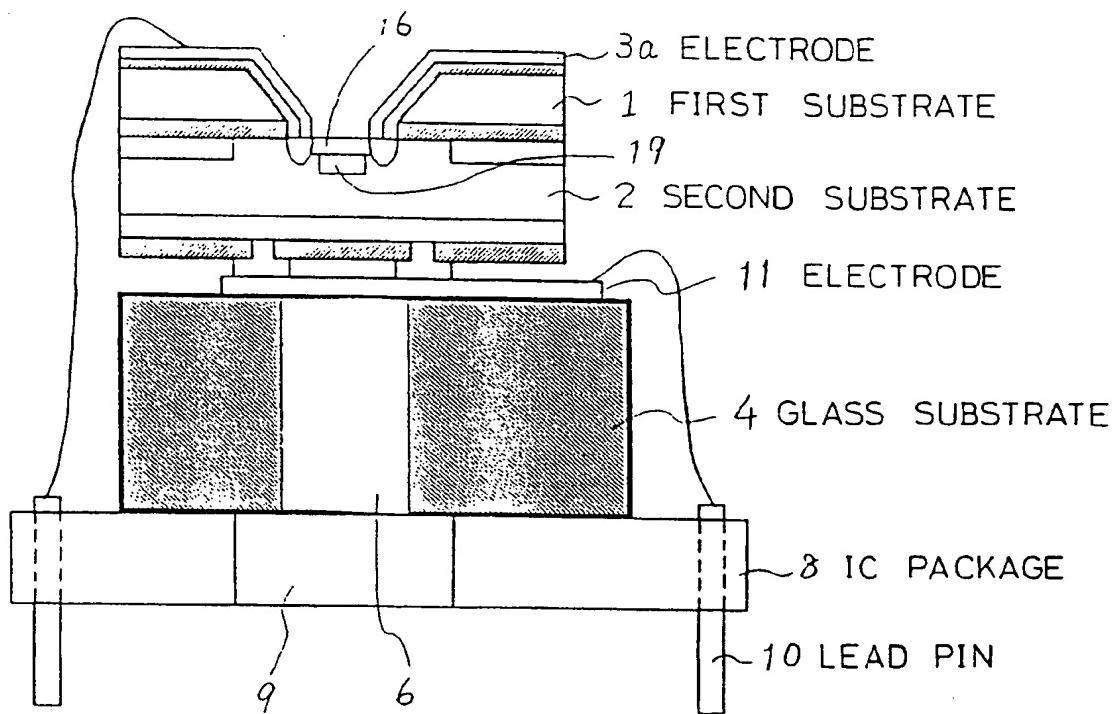


FIG. 17

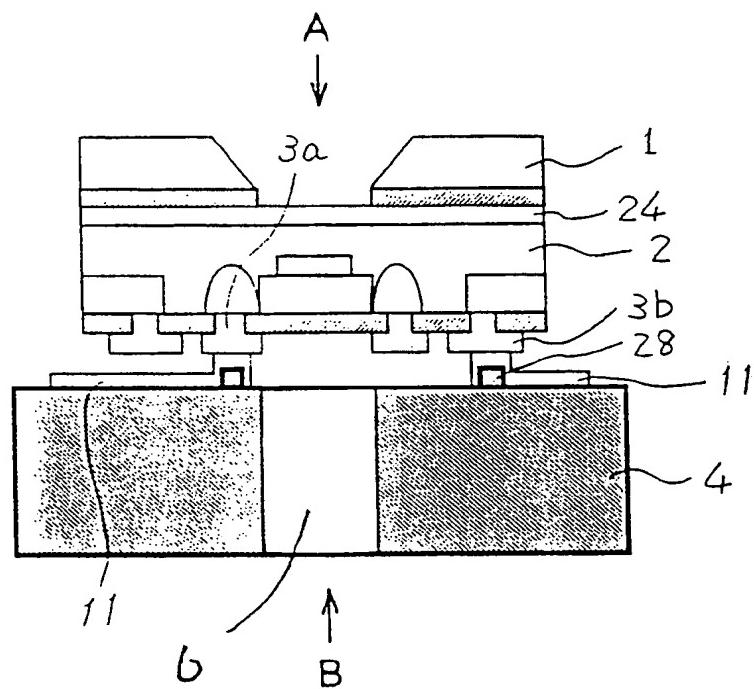


FIG. 18

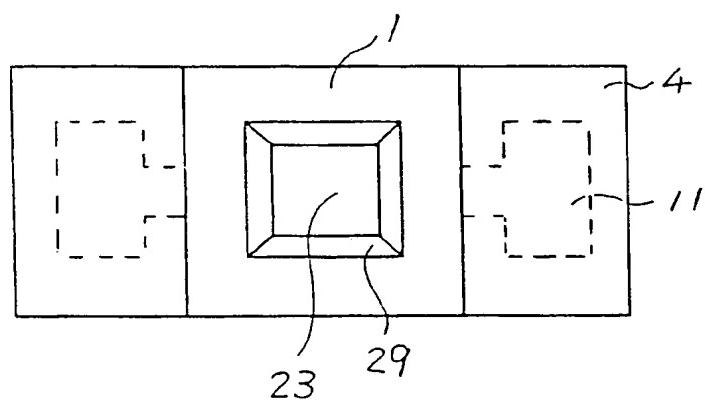


FIG. 19

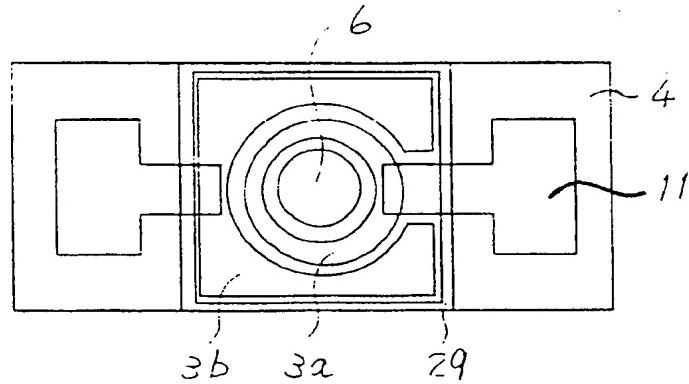


FIG. 20 PRIOR ART

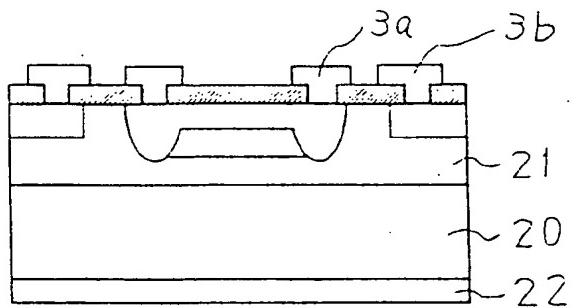


FIG. 21 PRIOR ART

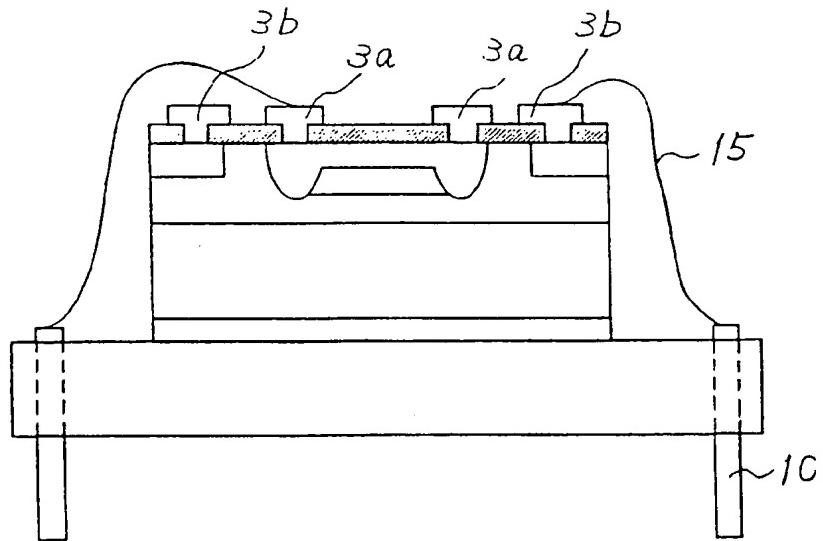


FIG. 22 PRIOR ART

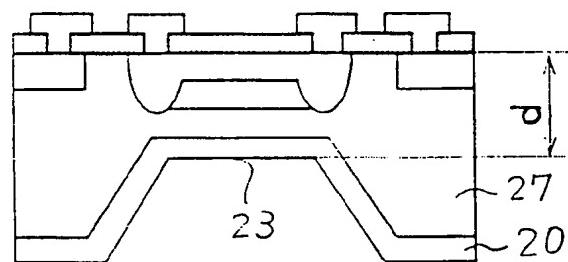


FIG. 23 PRIOR ART

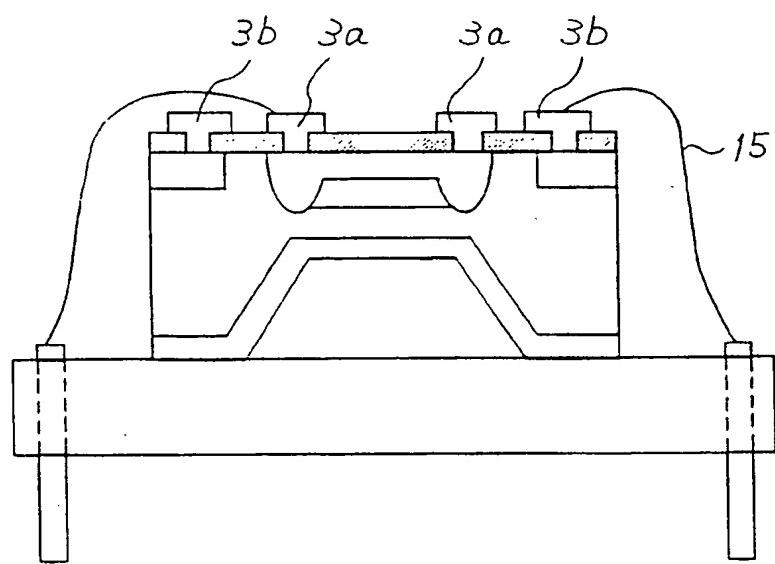


FIG. 24A

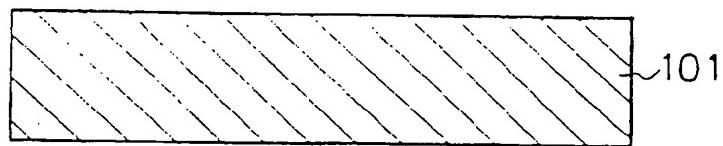


FIG. 24B

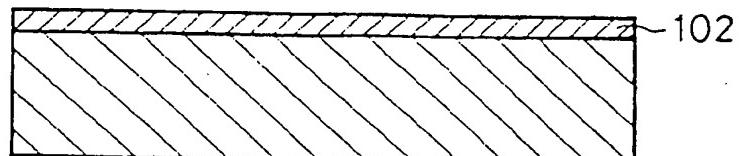


FIG. 24C

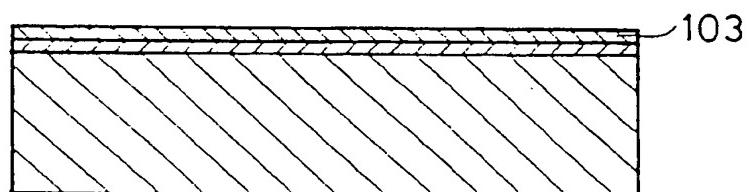


FIG. 24D

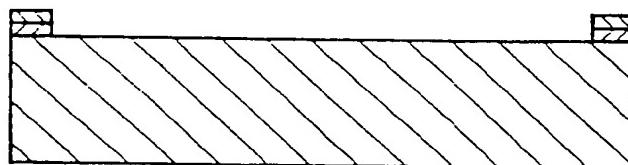


FIG. 24E

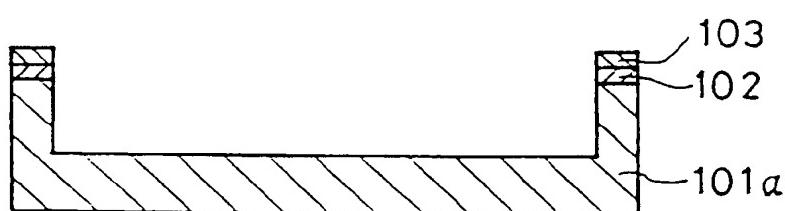


FIG. 24F

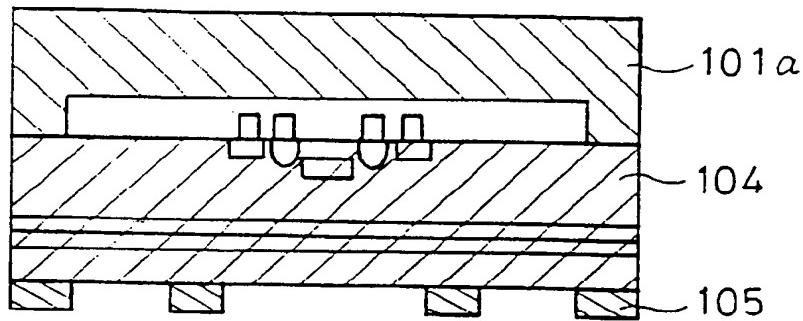


FIG. 24G

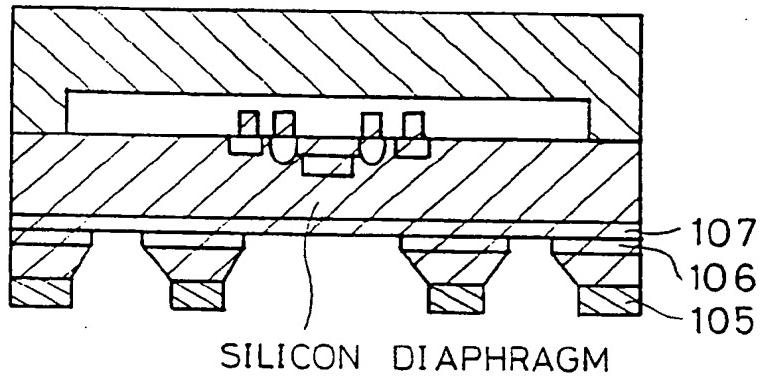


FIG. 24H

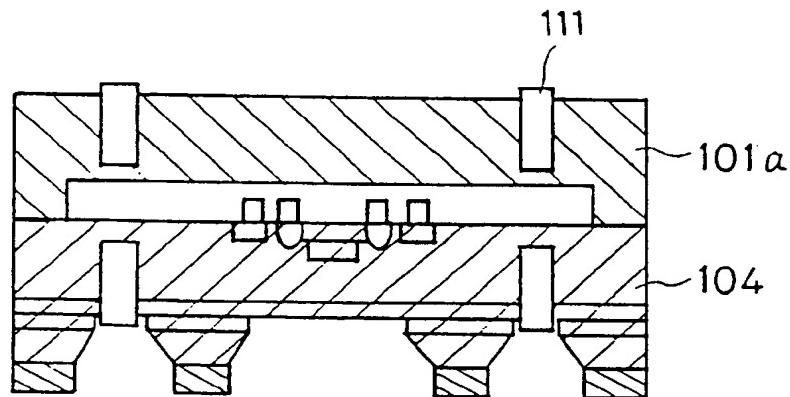


FIG. 24I

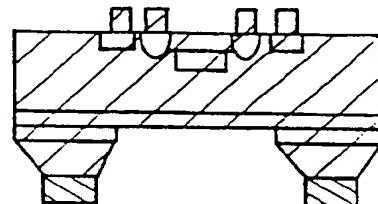


FIG. 25G

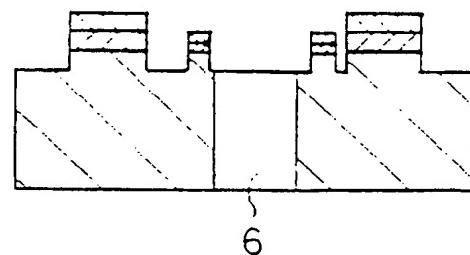


FIG. 25H

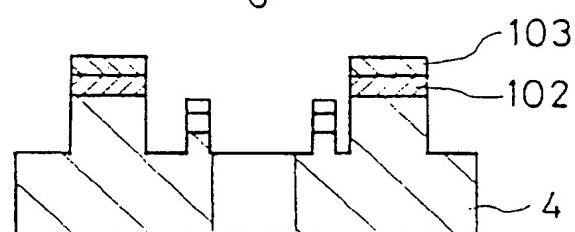


FIG. 25I

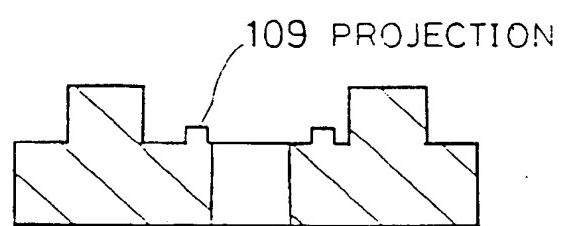


FIG. 25J

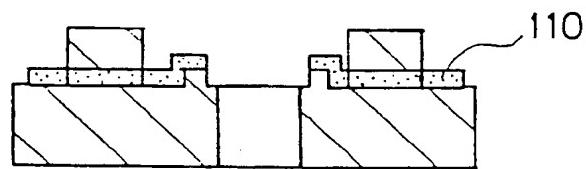


FIG. 25K

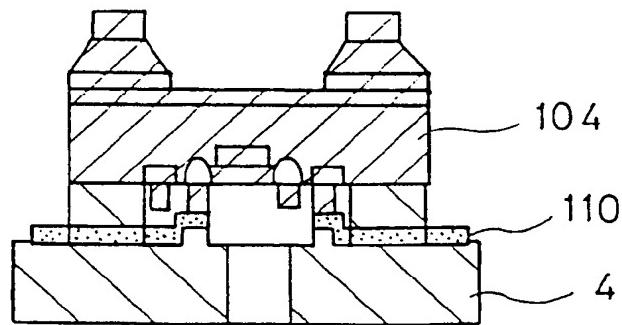


FIG. 25A

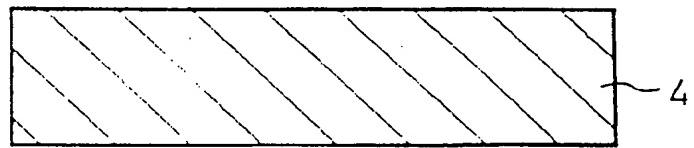


FIG. 25B

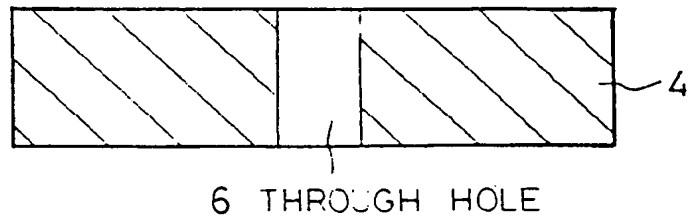


FIG. 25C

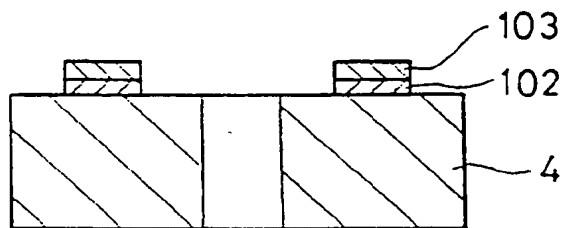


FIG. 25D

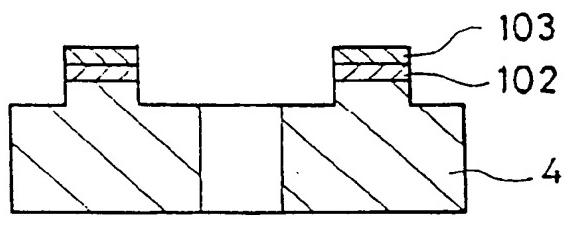


FIG. 25E

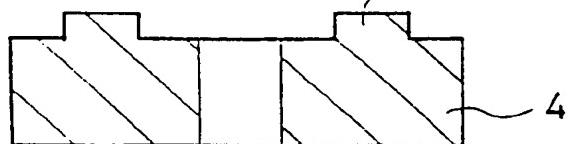
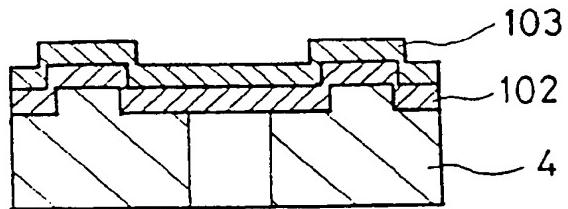


FIG. 25F





European Patent  
Office

## EUROPEAN SEARCH REPORT

Application Number  
EP 95 30 5733

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	FR-A-2 284 989 (COMP GENERALE ELECTRICITE) 9 April 1976 * figure *	1-8	H01L31/107 H01L31/0203
A	GB-A-1 441 261 (EMI LTD) 30 June 1976 * figure 5 *	1-8	
A	US-A-5 021 854 (HUTH GERALD C) 4 June 1991 * figure 7 *	1-8	
A	PATENT ABSTRACTS OF JAPAN vol. 014 no. 016 (E-872) ,12 January 1989 & JP-A-01 259539 (FUJITSU LTD) 17 October 1989, * abstract *	1,9,10	
A	PATENT ABSTRACTS OF JAPAN vol. 014 no. 210 (E-0922) ,27 April 1990 & JP-A-02 046770 (SEIKO EPSON CORP) 16 February 1990, * abstract *	1,9,10	
A	PATENT ABSTRACTS OF JAPAN vol. 004 no. 044 (E-005) ,5 April 1980 & JP-A-55 013963 (NEC CORP) 31 January 1980, * abstract *	1	TECHNICAL FIELDS SEARCHED (Int.Cl.6)  H01L
A	PATENT ABSTRACTS OF JAPAN vol. 015 no. 323 (E-1101) ,16 August 1991 & JP-A-03 120875 (YOKOGAWA ELECTRIC CORP) 23 May 1991, * abstract *	1,9,10	
A,P	EP-A-0 616 373 (SEIKO INSTR INC) 21 September 1994 * claims 18-28 *	1-8	
<p>The present search report has been drawn up for all claims</p>			
Place of search		Date of completion of the search	Examiner
THE HAGUE		14 November 1995	Lina, F
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X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons  & : member of the same patent family, corresponding document	